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10/032,058	12/31/2001	Katsuyuki Yonezawa	SON-2307	5643

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EXAMINER
ENGLUND, TERRY LEE

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,058	YONEZAWA, KATSUYUKI	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2001 and 06 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

Figures 13-15 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated (e.g. pages 1, 3, and/or 8-9 identify the figures as a "conventional example" of a first-order low-pass filter). See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The drawings are objected to because at least both Figs. 3 and 4 both show lines (e.g. with respect to when n=4) with small circles, and not the squares as cited on at least pages 16-17. If Fig. 6 shows circuits corresponding to those from Fig. 1, it is believed the reference characters of current sources "21B" and "22B" are reversed.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: It is not clear on lines 7-8 of page 2 how diodes Q2 and Q3 are connected in series with each other. As shown in Fig. 13, they coupled in parallel with respect to current source 112 and

ground 104. Page 26, lines 19-20 indicate elements Q36-Q39 are diode-connected. However, Fig. 9 shows they are parallel transistors within circuit 36A. On page 40, it is not understood what the descriptions "3-1: CONVENTIONAL CIRCUIT" and "3-2: CIRCUIT OF PRESENT INVENTION" relate to. For example, what do "3-1" and "3-2" mean? Appropriate corrections are required.

Claim Objections

Claims 1-9 are objected to because of the following informalities: It is suggested a comma be added after "transistor" on line 3 of claim 1, and after "diode" on line 9 of the same claim to minimize possible confusion. For example, as presently written, it appears the "one transistor and four diodes" of the first differential circuit are all coupled in parallel with respect to one another. However, it is only the diodes that are specifically connected in parallel with one another. Line 5 of claims 5 and 7 should have --point-- instead of "node" to correspond to the "common connection point" already recited within claim 1 (see lines 14-15). Claims 2-9 all carry over the objection from claim 1. Appropriate corrections are required.

Claim Rejections under 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 2 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make

and/or use the invention. It is not understood how a plurality of first (and second) differential circuits can be connected in series between first and second power supplies as recited within claim 2. It appears this claim corresponds to the applicant's Fig. 6. However, if each circuit has its respective first electrodes of the diode(s) and transistor(s) connected, where are those connections within the figure? For example, shouldn't the first electrodes (i.e. emitters) of Q11-1 and Q12-1 through Q15-1 be shown connected together? It appears only the first transistor of each first differential circuit of the plurality are connected in series with respect to each other, and the group of four parallel diodes of each first differential circuit of the plurality are connected in series with respect to each other. Without the first electrode connections, it doesn't appear there is a plurality of said first differential circuits (with the limitations of each first differential circuit as recited within claim 1) actually being connected in series.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3, 4, 6, 8, and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. It is not clear how the singular "second differential circuit" of claim 3 (line 6) can be connected in parallel to each of the plurality of first differential circuits. If claim 3 corresponds to the applicant's Fig. 7, then isn't there a corresponding second differential circuit in parallel with each first differential circuit? If not, the examiner requests to know which figure this claim's limitations refer to. It is not clear in claim 4 what "in series with each other" refers to on line 9. For

example, does it refer to the second differential circuits within the second series connection circuit, or to the first/second series connection circuits? The limitations within claims 6, 8 and 9 are misleading and/or indefinite. They appear to indicate each of the first/second differential circuits, and their current source, are also connected between other terminals. However, it is believed the circuits between the other terminals relate to circuitry that is similar to the first/second differential circuits and current source. For example, in the applicant's own Fig. 1, first circuit 15A, second circuit 16A, and current source 23A comprise a filter circuit between first input terminal 11 and first output terminal 18. However, they are not between second input terminal 12 and second output terminal 19 because circuits 15B/16B and current source 23B are positioned there. For similar reasons, how can the singular "capacitor" of claim 1 be coupled between the first circuit's input and output terminals, as well as between the second circuit's input and output terminals as claims 8 and 9 recite? If that is the case, which figure(s) reads on the "capacitor" related limitations recited within claims 8 and 9? It appears the limitations of claims 8 and 9 relate to the applicant's Fig 9 that actually shows capacitors 37A and 37B, not a single capacitor (e.g. 17) of the applicant's Fig. 1. Therefore, it is believed the limitations of claims 8 and 9 relate to two capacitors, and not the single capacitor recited within claim 1.

Claim Rejections under 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

In so far as being understood, claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mihailovits et al. (Mihailovits). Fig. 5 shows a doublet circuit, clearly related to a filter circuit as disclosed by Mihailovits, comprising a first differential circuit formed by one transistor 501, and diode-connected transistor 503 (having an emitter area n times larger than transistor 501); and a second differential circuit comprising one diode-connected transistor 504 and transistor 502 (having an emitter area n times larger than diode-connected transistor 504). Since diode-connected transistors 503 and 504 are commonly connected to current source IBIAS, their respective first/second currents will correspond to input signal Vin. Comparing Mihailovits' Fig. 5 circuit with the first/second differential circuits 15A/16A of the applicant's own Fig. 1, one of ordinary skill in the art would know Mihailovits': 1) first differential circuit 501,503,505 closely corresponds to the applicant's first differential circuit 15A (i.e. Q11,Q12-Q15,Q21A); 2) second differential circuit 504,502,506 closely corresponds to the applicant's second differential circuit 16A (i.e. Q20,Q16-Q19,22A); and 3) current source IBIAS corresponds to the applicant's 23A. Although Fig. 5 does not show a capacitor, one of ordinary skill in the art would realize from Mihailovits' figures and disclosure that Vout of Fig 5 would be connected to a capacitor (e.g. 240 of Fig. 2 connected to the common connection of diode-connected transistor 202 and current source 240). The reference does not clearly show/disclose the four parallel diodes within first differential circuit 501,503,505, nor the four parallel transistors within the second differential circuit 504,502,506, but the reference does clearly show/

disclose the differences in emitter areas with respect to the transistors and diode-connected transistors as previously described. Therefore, it would have been obvious to one of ordinary skill in the art to replace single diode-connected transistor 504 with a number n of parallel connected diode-connected transistors, and replace single transistor 502 with a number n of parallel transistors since it is well known that an n-number of parallel transistors/diode-connected transistors is functionally equivalent to a single transistor/diode-connected transistor that has an emitter area of n times the area of the single transistor/diode-connected transistor. Since Mihailovits clearly indicates the emitter areas are typically between 4 and 5 (see column 3, lines 45-49), and assuming a ratio of 4 was desired, it would have been obvious to one of ordinary skill in the art to replace Mihailovits' single diode-connected transistor 503 with four parallel diode-connected transistors, and single transistor 502 with four parallel transistors. With this configuration, current source IBIAS would be connected to a common connection point of the four diodes (diode-connected transistors) with respect to 503 of the first differential circuit, and the one diode (diode-connect transistor) with respect to 504 of the second differential circuit. Thus, the current through the corresponding capacitor (e.g. 240 of Fig. 1) would be determined by the current of current source IBIAS, the first current through the four diodes (corresponding to 503), and the second current through the single diode (corresponding to 504), rendering claim 1 obvious. The use of an n-number of parallel transistors (or diode-connected transistors) in place of a single transistor (or diode-connected transistor) having an emitter area of times that of a single device is well known to be functionally equivalent. Also, if a device of different

emitter area was desired, but not available, parallel devices having the same area could be used as a suitable substitution. Fig. 2 clearly shows a plurality of differential stages (i.e.. 260-280) connected in series between input Vin and output Vout. Each differential stage is also coupled between a first power supply (not labeled but identified as a voltage supply on column 2, line 17) and a second power supply (identified as ground on column 2, line 17). Therefore, replacing each differential circuit (e.g. 201,202,221, 222,246,240) within Mihailovits' Fig. 2 with a corresponding Fig. 5 circuit, claims 2-4 are rendered obvious. [From Fig. 5, it is understood that each first differential circuit 501, 503,505 has a corresponding second differential circuit 502,504,506. Therefore, there are an identical number of first and second differential circuits within the overall filter circuit of Mihailovits.] From Fig 5, one of ordinary skill in the art would know the control electrode of the single transistor 501, and the control electrodes of the four transistors (corresponding to 502) are connected to a first circuit input terminal (receiving input signal Vin), and the common connection point (i.e. between IBIAS and 503,504) is connected to a first circuit output terminal (for providing output signal Vout), wherein one terminal of the capacitor (e.g. 240 of Fig. 2) would be coupled to the first circuit output terminal, rendering obvious claim 5. Coupled to the other terminal of capacitor 240, is a corresponding circuit 203,204,223,224,247,241. Since this corresponding circuit can also comprise Fig. 5's first/second differential circuits (with parallel transistors and diode-connected transistors as described previously) and current source, claim 6 is rendered obvious. With each of the differential pairs of Fig. 2 replaced with the modified circuit of Fig 5, as previously described, claims 7-9 are also rendered obvious as

described below. One of ordinary skill in the art would recognize the bases of transistors 201 and 204 as receiving differential input Vin. However, it would have been obvious to one of ordinary skill in the art to connect one of the control electrodes (i.e. base) of transistors 201 and 204 (e.g. 204) with a direct-current power supply, such as a reference voltage. Deeming the right side of capacitor 240 (connected to the common connection node of diode 203 and current source 241) as a first circuit output terminal, and the base of transistor 201 as a first input terminal, capacitor 240 is coupled between them, rendering obvious claim 7. The input signal to the base of transistor 201 would be compared to the direct-current power supply applied to the control electrode of transistor 204. This would allow the ability to select a predetermined reference point for when the filter/differential circuit would trigger with respect to the input signal received by the overall circuit. Similarly, deeming the left side of capacitor 240 (connected to the common connection node of diode 202 and current source 240) as a second circuit output terminal, and the base of transistor 204 as the second input terminal, capacitor 240 is also coupled between them, rendering obvious claim 8. Also, interpreting the base of transistor 201 of Fig. 2 (corresponding to the control electrodes of Fig. 5's transistors 501 and 502) as the first circuit input terminal, the common connection point between 240 and 202 (corresponding to the common connection point between IBIAS and 503,504 of Fig. 5) as a second circuit output terminal, the base of transistor 204 of Fig. 2 (corresponding to the control electrodes of Fig. 5's transistors 501 and 502) as the second circuit input terminal, and the common connection point between 241 and

203 (corresponding to the common connection point between IBIAS and 503,504 of Fig. 5) as a first circuit output terminal, claim 9 is rendered obvious.

No claim is allowable.

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed invention. Fig. 2 of Koyama et al. shows an example of first/second differential circuits 140/150, each having a single transistor (151/153), and a transistor (152/154) with multiple emitters (thus being equivalent to multiple transistors connected in parallel) for improved linearity. Although none of the transistors are clearly shown or disclosed as being diode-configured, Koyama et al. does disclose transistors 152 and 153 each have an emitter area that is four times larger than transistors 151 and 153 (see column 1, lines 55-57). [That description is believed to be incorrect, since one of ordinary skill in the art would realize the areas of multi-emitter transistors 152 and 154 shown in Fig. 2 would typically be larger than those of corresponding transistors 151 and 153.] Okanobu shows examples of parallel transistors Q21-Q24 (e.g. Fig. 5) and a corresponding single transistor Q2'(Q4') (e.g. Fig. 6) with a larger emitter area. Column 5, line 64 through column 6, line 18 explain their relationships, and clearly identify the number of transistors and/or emitter area ratio as 4 (see column 5, line 65; column 6, lines 4-5,9, 12, 13, and 14). Figs. 7 and 8 of Shoji et al. is structurally identical to the applicant's own Figs. 15 and 13, respectively. [Co-inventor Yonezawa of that reference is the inventor of the present application.] Although not used in any formal rejections described above, it is noted that the teachings of Mihailovits' filter circuit provides motivation to replace each differential pair (e.g.

Q1,Q2,25) of Shoji et al.'s Fig 8 with a corresponding differential circuit as shown in Mihailovits' Fig. 5. Therefore, all of these references should be carefully reviewed and considered.

If the applicant wants Japanese Patent Laid-Open Hei 9-69752 (cited on page 1 of the disclosure) considered and cited if the application is issued as a patent, the examiner requests a copy of that reference, and a corresponding IDS.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (703) 308-4817. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax number for TC 2800 is (703) 872-9318 for communications before a final action has been mailed, and (703) 872-9319 for communications after a final action.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

TLE
Terry L. Englund

27 September 2002

TIMOTHY P. CALLAHAN
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